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Academic Experience

Ph.D. in Electrical and Computer Engineering
Thesis: *Adaptively Quadratic (AQua) Image Models and Their Applications*.
Advisor: Professor Thomas W. Parks
Cornell University, Ithaca, New York. May 2002.

Master of Electrical Engineering (3.9/4.0)
Thesis: *Orthogonal, Exactly Periodic Subspace Decomposition.*
Advisor: Professor Thomas W. Parks
Cornell University, Ithaca, New York. Spring 1997.

B.S. in Electrical Engineering (3.7/4.0)
Senior Thesis: *Design and Implementation of a PC Oscilloscope.*
Advisor: Professor Paul Schimpf
University of Washington, Seattle, Washington. Spring 1996.

B.S. with Distinction in Mathematics (3.8/4.0)
Senior Thesis: *Theorems on Global Univalence.*
Advisor: Professor Tom Duchamp
University of Washington, Seattle, Washington. Spring 1996.

Honors

Howard A. Acheson Scholar: Cornell University, Ithaca NY.
Teaching assistantship from Cornell University College of Engineering. Fall 1996.

Electrical Eng. Open House Certificate of Recognition: University of Washington, Seattle, WA.
Awarded 4th prize for Outstanding Technical Exhibit for the design and implementation of a 12MHz PC-Oscilloscope. (The Oscilloscope consisted of both: hardware PC card and Windows software.) Recognized as the only placing undergraduate exhibit out of thirty graduate and undergraduate entries. Spring 1996.

Math Research Experience for Undergraduates (REU): University of Washington, Seattle, WA.
Active participant in a theoretical math research program sponsored by the National Science Foundation. Authored original paper addressing the relationship between networked resistors and boundary currents and potentials. Summer 1993.

Academic Honor Associations: Eta Kappa Nu (HKN), IEEE and Golden Key National Honor Society.

Work Experience

Chief Software Architect: Leidos, formerly SAIC, Alexandria VA.
► 2010–Present, Program Manager: Support IR&D programs focused on streaming LIDAR data, real-time LIDAR processing, and Geiger mode LIDAR processing.
► 2010–2013, Chief Software Architect/Principal Investigator: Principal investigator on the graphics processing unit (GPU) ortho-rectification tool delivered as part of the Operational 3D (Op3D) Joint Capability Technology Demonstration (JCTD). Supported research into new image, full-motion video, and LIDAR compression algorithms. The work on full-motion vision compression was in support of the U.S. Marine Corps. Was a consultant for the Leidos team that performed LIDAR compression work for AFRL (RDUCE).
► 2009–2010, Principal Investigator: Supported DARPA seedling and lead software engineer on AGC's Op3D JCTD program. Developed a flexible 3D data compression architecture and application. The architecture can ingest Digital Elevation Model (DEM) and LIDAR, compressing it at different user-defined rates and resolutions. The extensible framework was available to third-party applications and was integrated into TerraGo's 3D GeoPDF tools as part of the Op3D JCTD program.

Work Experience

► 2006–2007, System Architect: Supported Buckeye's real-time unmanned aerial vehicle (UAV) processing architecture. Developed a real-time, multithreaded processing architecture that controls the electro-optical (EO) data processing and transmission onboard the UAV Buckeye system. The current Buckeye UAV system collects LIDAR and EO imagery. EO imagery is processed and transmitted to ground in real time. The data processing architecture is very flexible with support for load balancing and easy expansion through the use of processing plugins.
► 2004–2007, System Architect: Supported DARPA's 3DF (Phase 4 of E3D) LIDAR-based vehicle recognition system. The system classified and fingerprinted personal occupancy vehicles from 3D and 2D sensor data. Developed the LIDAR collection and raw conversion software and was the lead architect for the overall processing architecture. The real-time prototype system was demonstrated successfully at the U.S. Army Topographic Engineering Center.
► 2004–2007, Principal System Integrator: Supported DARPA's UrbanScape and AGC's UrbanRecon programs. Developed a vehicle-based, integrated real-time prototype system for creating 3D models of urban areas and fusing them with aerial data. Successfully demonstrated the ability to generate 3D model aerial data fusion. Developed the LIDAR, inertial navigation system (INS), and camera synchronization hardware that received the Patent No. 7,752,483 B1, July 2010. Developed the core processing and synchronization hardware and software and was the lead for all the data processing software.

Chief Technology Officer: Van Gogh Imaging, Inc. (VGI), Springfield VA.
► Developed an arm based 3D scanning and registration system and a 360 view imaging system. October 2007 – March 2009.

Signal Processing Analyst: Solers, Arlington, VA.
► Acted as a Scientific, Engineering, and Technical Assistance (SETA) consultant for Defense Advanced Research Projects Agency (DARPA). While at Solers, I supported the "Exploitation of 3-D Data" program (E3D) managed by Dr. Robert A. Hummel. July 2003 – November 2004.

Founder of Digital Multi Media Design - DMMD: Arlington, VA.
► Founder of start-up company developing novel image and signal processing software used in commercial, agricultural, veterinarian and medical applications. Duties include developing image processing algorithms, marketing products and services, and seeking investment opportunities. WhiteCap, one of DMMD's DICOM viewers, has been FDA approved. More information about DMMD can be found at http://www.dmmd.net. September 2002 – present

Research Assistant: Cornell University, Ithaca, NY.
► Primary research investigator for Prof. Thomas W. Parks' DSP Lab at Cornell University. Texas Instruments, NSF, ONR and Kodak sponsored our innovative work on Digital Image Processing. Fall 1996 – Spring 2002.

Technical Journal Reviewer: Cornell University, Ithaca, NY.
► Reviewer for *IEEE Journal on Signal Processing,* and *IEEE Journal on Image Processing,* and *Computer Vision and Image Understanding*. 1999 – Present.

Hardware Design Engineer: Hewlett Packard (Agilent), Rohnert Park, CA.
► Redesigned and implemented the Fast Analog to Digital Conversion board (option 7) for improved peak/pit detection in the new, flat panel display, HP 8560 E Series Spectrum Analyzer. My original design became part of the final product. May 1998 – Aug. 1998.

Software and Hardware

OS, Software Tools, and Network Protocols:
Intermediate to advanced working knowledge of: UNIX, LINUX, Microsoft Windows (all versions), Matlab (+Mex files), PSPICE, Verilog, Visual C++ (Win32 API), C#, MASM (assembly language), HTML, CGI, and TCP/IP network protocol.

Hardware Chips:
Intermediate to advanced working knowledge of: Altera, ACTEL, and Xilinx FPGA chips and their corresponding hardware development tools. Advanced knowledge of interfacing to IBM personal computers and a working knowledge of Intel, Motorola, and TI DSP processors. Also expert knowledge of A/D, D/A, and PLL design.

Citizenship

US Citizen: Naturalized since 1994.

Activities

Avid player and organizer of recreational soccer leagues. I enjoy swing and Latin dancing, DJing, board water diving, cross-country bicycle tours, running (1997 Marine Corps Marathon) and roller-skating.

References

Available Upon Request

Journal Publications

[1] D. D. Muresan and T.W. Parks*, Orthogonal, Exactly Periodic Subspace Decomposition,* IEEE Journal On Signal Processing. , Sept. 2003 Page(s): 2270 -2279.
[2] D. D. Muresan and T. W. Parks, *Adaptively Quadratic (AQua) Image Interpolation*, IEEE Journal on Image Processing, May 2004, Volume 13, Number 5, Pages: 690-698.
[3] D. D. Muresan and T. W. Parks, *Demosaicing Using Optimal Recovery, I*EEE Journal on Image Processing, February 2005, Volume 14, Number 2, Pages: 267-278.

Conference Publications

[1] D. D. Muresan, *Fast, Adaptively Quadratic Image Interpolation, International Conference on Image Processing, Genoa, Italy 2005.*
[2] D. D. Muresan and T. W. Parks, *Adaptive Principal Components and Image Denoising,* IEEE International Conference on Image Processing (ICIP), Barcelona 2003.
[3] D. D. Muresan and T. W. Parks *Optimal Face Reconstruction Using Training*, IEEE International Conference on Image Processing (ICIP) 2002, Rochester, NY.
[4] D. D. Muresan and T. W. Parks *Optimal Recovery Demosaicin*g, IASTED Signal and Image Processing, Hawaii 2002.
[5] D. D. Muresan and T.W. Parks *Optimal-Recovery Approach to Image Interpolation,* IEEE International Conference on Image Processing (ICIP), Greece, 2001.
[6] D. D. Muresan and T.W. Parks *Adaptive, Optimal-Recovery Image Interpolation,* IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), Salt Lake City, Utah, 2001.
[7] K Kinebuchi, D. D. Muresan, and T.W. Parks *Image Interpolation using Wavelet-Based Hidden Markov Trees*, IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), Salt Lake City, Utah, 2001.
[8] D. D. Muresan and T.W. Parks *Prediction of Image Detail,* IEEE International Conference on Image Processing (ICIP), Vancouver, 2000.
[9] D. D. Muresan and T. W. Parks *A New Approach to Period Estimation*, IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), Turkey, 2000.
[10] D. D. Muresan and T. W. Parks *Orthogonal Subspace Decomposition of Periodic Signals*, Conference Record of the Thirty-Third Assilomar Conference on Signals, Systems and Computers, 1999

Workshop Publications

[1] D. D. Muresan and T. W. Parks *Image Interpolation Techniques Using Adaptive Linear Functions and Domains*, IEEE Western New York Image Processing Workshop, 2001.
[2] D. D. Muresan and T. W. Parks *New Image Interpolation Techniques*, IEEE 2000 Western New York Image Processing Workshop, Oct. 13, 2000.
[3] D. D. Muresan, Steve Luke, and T. W. *Parks Reconstruction of Color Images from CCD Arrays*, Texas Instruments DSP Fest, Houston TX, August 2000.
[4] D. D. Muresan, Ashish Raj, Harold K. Figueroa and T. W. Parks *Review of Image Interpolation Techniques*, IEEE Western New York Image Processing Workshop, 1999.
[5] D. D. Muresan and T. W. Parks *Orthogonal Subspace Decomposition Of Periodic Signals*, Texas Instruments DSP Fest, Houston TX, August 1999.

Technical Reports

[1] D. D. Muresan *Review of Optimal Recovery*, DSP Lab at Cornell University, Technical Report TR-2002-10. (http://dmmd.net/research/publications/tr/or.pdf)
[2] D. D. Muresan *Notes on Perfect Reconstruction Filter Banks II*, DSP Lab at Cornell University, Technical Report TR-2001-10. (http://dmmd.net/research/publications/tr/pr.pdf)
[3] D. D. Muresan, *Intuitive Linear Algebra Review*, DSP Lab at Cornell University, Technical Report TR-2000-10. http://dmmd.net/research/publications/tr/matrix.pdf)

Inventions

[1] Apparatus For Recording and Playback of Multi-dimensional Data, Patent pending, November 2008.

[2] Apparatus for Compressing Multi-dimensional Data Using Sensor Pose and Position Information, Patent pending, November 2008.

[3] Apparatus for Extracting and Registering 3D Data Using a Single Digital Camera and Fiducials, Patent pending Feb. 2009.

[4] Apparatus For Recording 3D Data Using a 2D Camera and Rotating Table, Patent pending, March 15, 2009.

[6] D. Darian Muresan and Andrew Weitz *Real Time 3D Vehicle Based LIDAR Scanning System,* Patent No. 7,752,483, July 6, 2010.

[7] D. Muresan and D. Darian Muresan *Multi-Flash Analog to Digital Converter Using Floating Voltages,* Patent No. 6,091,346, July 18, 2000.

[8] D. Darian Muresan and D. Muresan *Procedure to Attach a Lamp on the Ceiling*, Patent No. 6,609,692, August 2003.

[9] D. Darian Muresan and D. Muresan *Fast Edge Directed Polynomial Interpolation*, Patent No. 7,212,689 B2.

[10] D. Darian Muresan and D. Muresan *Computer Mouse*, Patent No. 7,015,895.

[11] D. Darian Muresan and D. Muresan *Synchronized Processing of Views and Drawing Tools In a Multiple Document Interface Application*, Patent pending, 2003.

[12] D. Darian Muresan *Fast Edge Directed Demosaicing*, Patent No. 7,525,584 B2.

[13] D. Darian Muresan and D. Muresan *Moving-Pixel Procedure for Digital Picture Edge-Smoothing Procedure for Digital Picture Edge-Smoothing* Patent No. 6,885,383.

Hardware Experience

My current hardware experience is based on the development of several different data acquisition systems, a patent for a multi-flash analog to digital converter and a patent for a 3D Vehicle LIDAR Scanning system.

My most recent hardware project was the development of a multi-sensor timing integration board for a 3D urban scanning system. The final design consisted of integrating multiple LIDAR scanners, digital cameras, video cameras and INS (inertial navigation system) sensors into a synchronized scanning system that could scan a city block in real-time. The patent for this system is Patent No. 7,752,483, July 6, 2010. I am the primary author.

Other hardware design projects are listed in chronological order:

My first hardware project was my senior project at University of Washington. It was the design of a 10 MHz PC oscilloscope that used the XT card slot. The oscilloscope was designed from discrete TTL logic and it contained two unique features. The first feature was the implementation of a ping-pong memory. Data from the analog to digital converter (ADC) was written to one memory bank, while the PC read the data from a second memory bank. When the PC finished reading the data, the memory banks were switched. This way the data was always available for display. A second unique feature was the implementation of a hardware based over-sampling scheme where under certain conditions, the oscilloscope could sample data at frequencies higher than the sampling frequency of the ADC. In the 1996 *Electrical Eng. Open House* competition held at University of Washington, my project was recognized as the only placing undergraduate exhibit out of thirty graduate and undergraduate entries.

My second project was the hardware design that I have done on a synchronous data acquisition system used in my graduate work on *preventive maintenance.* The card was an ISA based PC card and the digital logic was implemented on an Altera programmable gate array (PGA). The unique feature of this data acquisition system was that data was being sampled based on the positions of the gears in the gearbox. The period estimates of the vibration data were then displayed on the PC. My theoretical work and results on this project are summarized in a journal paper entitled *Orthogonal, Exactly Periodic Subspace Decomposition*, which appeared in the IEEE Journal on Signal Processing in 2003.

Hardware Experience

My third project was implemented during the 1998 summer internship at Hewlett Packard (HP) where I redesigned the *Fast Analog to Digital Conversion board (option 7)* which improved peak/pit detection in the new, flat panel display, HP 8560 E Series Spectrum Analyzer. The entire digital logic was done using Verilog and was programmed into an Actel FPGA chip. At the end of the internship HP was so satisfied with my progress that upon my request HP donated thousands of dollars worth of test equipment to Prof. Parks' DSP Lab at Cornell University. Later I learned that my original design became part of the final HP product.

My fourth hardware development project was the design of a multi-flash Analog to Digital Converter. The ADC has been patented in the USA under the US patent number 6,091,346.

Software Experience

My current job is Chief Software Architect at Leidos. In this position I am in charge of overseeing most of the software design projects and encouraging good software design processes (such as the Unified Process) and practices. I was the lead software designer for the image processing pipeline for Buckeye – an army program that was featured in a CNET article: "Army Touts Top Tech Inventions:"

Before joining Leidos, I founded Digital Multi-Media Design (DMMD) where I am currently the Chief Technology Officer and software architect. DMMD is a 3D/2D image processing and visualization software company that develops medical, industrial and consumer software for capturing, processing, editing and managing 3D/2D images.

DMMD has developed several image processing applications used in consumer and medical applications. Some of these projects are: Visere, WhiteCap, eVet Viewer, Exuo, Algorithms Signal Processing Library (DMA), Vincent, and ShutterStream. Visere, WhiteCap and ShutterStream are enhanced image viewing and management tools containing patented algorithms for image interpolation, denoising, and demosaicing. Exuo is a PACS based server (used for storing and retrieving medical DICOM images) and DMA is a parallelized signal processing library. Additionally, DMMD provides software customization, patent licensing, consulting, and programming outsourcing to third party customers such as:

- LifeSize (http://lifesize.com)
- Pictometry (http://pictometry.com)
- SAIC (http://saic.com)
- SimonDr (http://www.simondr.com)
- eVet Diagnostics (http://www.evetdiagnostics.com)
- Van Gogh Imaging (http://www.VanGoghImaging.com)
- Pixido Imaging (http://www.pixido.com)
- Prairie Seating Corporation (http://www.prairieseating.com)
- And others